HIGH SPEED DIGITAL SYMPOSIUM

Call for Papers

High Speed Digital Symposium, a special session at EDI CON

Thursday, October 18, 2018

This year's topic: Life at the Edge: Delivering >100 Amps with less than 10 mV of noise to digital devices

Many high performance computing devices are power hogs. Some boards with high end microprocessor or graphics processor or FPGA devices require more than 100 Amps of current. But, with core voltage levels shrinking, this means noise margins are shrinking and the acceptable noise must be below 10 mV in some applications. This is a target impedance below 100 uOhms, to high bandwidth. The challenges of converting the power distribution bus voltage down to such low levels, while delivering high currents and high current transients while maintaining low voltage fluctuations, is the topic of this year's High Speed Digital Symposium on Thursday, October 18.

As with the previous year, we invite experts in the field to present application case studies of how they have implemented >100 A, low noise power distribution systems, or applied new techniques to design, test, or characterize these demanding applications.

Each of the five presentations in this session will be 20 minutes long, then 10 min of question and answer. At the end of the presentations, each speaker will be invited back to a panel discussion led by Eric Bogatin to dive deeper into the problems and solutions facing power engineers living at the edge.

Only slides are required for this special session, but presenters will be invited to write an article for the SI Journal on their topic.

Deadline for abstract submission is May 31. Selection will be made by June 15.

Submit abstracts here:

http://www.ediconusa.com/callforpapers.asp

Specify the track: High Speed Digital Symposium

EDI CON 2018 Electronic Design Innovation Conference & Exhibition

Where high frequency meets high speed.